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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,460	12/29/2003	Robert M. Ellis	42P18460	7056

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EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

21C

Office Action Summary	Application No.	Applicant(s)	
	10/748,460	ELLIS ET AL.	
	Examiner	Art Unit	
	Huan Hoang	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-7,14-16 and 24-32* is/are allowed.

6)☒ Claim(s) *1-3,8-11 and 17-21* is/are rejected.

7)☒ Claim(s) *4,12,13,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-4 and 19-23 are objected to because of the following informalities:

The word "retrieve" (claim 1, line 15 and claim 19, line 21) should be "retrieved". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8, 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The recitation "wherein the second logic is comprised of refresh logic control the at least a portion of the first logic ..." (claim 8 and claim 17, lines 1-2) is confusing since it is unclear what the subject of verb "control" is and what control the at least a portion of the first logic.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-3 and 9-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Hikada et al..

Hikada et al. discloses a DRAM IC having all the elements as recited in claims 1-3 and 9-11 as follows:

a first external connection (12, Fig. 1) to receive a first power supply voltage (Ext.Vcc2);

a second external connection (10, Fig. 1) to receive a second power supply voltage (Ext.Vcc1) that is lower than the first power supply voltage (column 9, line 20 and column 9, line 24);

a plurality of memory cells (102, Fig. 1) organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage (via circuit 106, Fig. 1);

a first logic (inverter of Fig. 3 for row decoder 124, Fig. 2 and column 10, lines 42-44) directly coupled to the memory cells to at least transmit signals to the memory cells (column 10, lines 30-34), wherein the first logic is powered by the first power supply voltage (via circuit 108, Fig. 1);

a second logic (200, Fig. 1 and Fig. 2) coupled to the first logic (via address buffer and row predecoder, Fig. 2) to produce an external interface to receive commands and addresses to select memory cells, and to both received data to store

within and output data retrieved from the selected memory cells, wherein the second logic is powered by the second power supply (Fig. 2);

wherein the first logic is coupled to the plurality of bit lines, and both transmits data across the plurality of bit lines to the plurality of memory cells and receives data from across the plurality of bit lines from the memory cells (column 10, lines 30-34);

wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells

A circuitboard and a plurality of electrical contacts recited in claims 9-11 are inherent in an integrated circuit.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikada et al. in view of Forbes et al.

Hikada et al. discloses all the limitations of claims 19-21 (Figs. 1, 2 and 3) except for a processor coupled to a memory controller. However, Forbes et al. (Fig. 4 and column 6, lines 27-30) discloses a memory controller (410) coupled to a processor (401) for controlling the operation of memory (400) in response to control signals received on control lines 416 from the processor (401). It would have been obvious to one having

ordinary skill in the art at the time the invention was made to use a memory controller coupled to a processor to control the operation of a memory device.

Allowable Subject Matter

8. Claims 5-7, 14-16 and 24-32 are allowed.

9. Claims 4, 12, 13, 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 8, 17 and 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or suggest the following:

the first logic is comprised of refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the DRAM IC is placed in a lower power state in which the second logic is deprived of power as a result of the second power supply voltage being removed.

a third logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from

the selected memory cells, wherein the third logic is powered by the third power supply voltage.

signaling a memory device to enter into a lower power state;

depriving the second logic of power by removing the second power supply voltage;

carrying out at least one refresh operation wherein the first logic signals a row of the plurality of the memory cells through a word line to which the row of the plurality of memory cells and the first logic are coupled;

restoring the second power supply voltage to the second logic by providing the second power supply voltage; and

signaling the memory device to exit the lower power state.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Mon-Fri 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Huan Hoang
Primary Examiner
Art Unit 2827

HH
3/30/05.